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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/029,146	12/28/2001	Kyo Seop Choo	465-884P	5228

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EXAMINER
QI, ZHI QIANG

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 09/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/029,146	CHOO ET AL.	
	Examiner	Art Unit	
	Mike Qi	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4,6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-18 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 8-14 of U.S. Patent No. 6,466,280 in view of US 6,528,357 (Dojo et al).

Although the conflicting claims are not identical, but they are not patentably distinct from each other because the claims 8-14 of the patent US 6,496,238 have a very corresponding limitations claimed in the claims 1-18 of this application, and substantially they have the doctrine of obviousness-type double limitations. Especially, the claims 1 and 13 claimed the limitations for the input line (electrodes) arrangement for an LCD device are covered by the claims 8-14 of the patent US 6,466,280.

For example, claims 1 and 13 of this application claimed an LCD and the method of for manufacturing an LCD having a cell array region and an input line part comprising:

(concerning claim 1 and 13)

- a first line layer (gate line) formed on a substrate;
- a first insulating layer (gate insulating layer) formed on the substrate, having a contact hole therein located at the first line layer;
- a second line (data line) formed on the first insulating layer;
- a second insulating layer formed on the substrate, having respective contact holes therein located at the first and second line layers (the gate line and the data line layers);
- a third line layer (reflective electrode) formed on the second insulating layer;
- a passivation layer (a third insulating layer) formed on the substrate, having respective contact holes therein located at the first, second and third line layers (the gate line, date line and the reflective electrode);
- a pixel electrode on the passivation layer (the third insulating layer) to electrically connect the first, second and third line layers (the gate line, data line and the reflective electrode) through each contact hole;

(concerning claim 13)

- a semiconductor layer formed on the first insulating layer of the cell array region.

The claim 8 of the patent US 6,466,280 claimed a transflective LCD device comprising a second substrate having:

- a gate electrode (gate line) formed on the second substrate;

- a first insulating layer (gate insulating layer) formed on the exposed surface of the second substrate while covering the gate electrode;
- a semiconductor layer formed on the first insulating layer . . .;
- a source electrode and a drain electrode (forming the data line) overlapping one end portion of the semiconductor layer (also means the data line formed on the gate insulating layer);
- a second insulating layer formed the exposed surface of the first insulating layer while covering the source and drain electrode, having contact hole (also means the second insulating layer formed on the substrate and having contact hole);
- a reflective electrode (as a third line layer) formed on the second insulating layer . . .;
- a third insulating layer (such as a passivation layer) on the reflective electrode and having contact hole (also means a passivation layer formed on the substrate and having contact hole);
- a pixel electrode formed on the third insulating layer and electrically connected with the reflective electrode through contact hole.

Therefore, the claims 1 and 13 of this application and the claim 8 of the patent US 6,466,280 substantially have the doctrine of obviousness-type double limitations, and they have at least an obviousness-type difference.

Claim 2, the gate line is the first line layer, inherently, the material of the first line layer is the same as the gate line, and that would have been at least obvious.

Claim 3, Dojo discloses (col.3, lines 59-67; Fig.2) that the scanning line (111) have a double-layer structure consisting of Aluminum-Neodymium (AlNd) alloy film (1110) and molybdenum (Mo) film (1111). Dojo indicates (col.2, lines 52-68) that due to such multi-layer formation (the scanning line comprised such Al alloy) would lower the wiring resistivity and would have no damage from etching process. Therefore, it would have been obvious to those skilled in the are at the time the invention was made to use AlNd and Mo double layer to form the gate line as claimed in claim 3 for reducing the line resistance and secure the line formation have no damage from the etching process.

Claims 4 and 5, the data line is the second line layer, inherently, the material of the second line layer is the same as the data line, and using metal Cr that is common and known in the art, because the metal Cr has a high corrosion resistance.

Claims 6 and 7, the reflective layer (reflective electrode) is the third line layer, inherently, the material of the third line layer is the same as the reflective layer, and Dojo discloses (col.8, lines 39-42) that the AlNd alloy is a low-resistance material. Therefore, using AlNd alloy as the material of the reflective layer would reduce the line resistance and the metal material comprising Al alloy having high reflectance, and that is common and known in the art. Therefore, it would have been obvious to those skilled in the art at the time the invention was made to use AlNd alloy as the material of the reflective layer as claimed in claims 5 and 6 for reducing the line resistance and having high reflectance.

Claims 8-9 and 14-15, the limitations are only given weight as intended use as the gate line, data line, reflective electrode, and the insulating layers can be used in a

reflective LCD or a transflective LCD and that is dependent on the different applications, and that would have been at least obvious.

Claims 10-12 and 16-18, concerning the first insulating layer, the second insulating layer and the passivation layer (third insulating layer) formed on an entire surface of the substrate are covered by the claims 1 and 13 of this application and also covered by the claim 8 of the patent US 6,466,280 and as shown in the Fig.5E.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Qi whose telephone number is (703) 308-6213.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

ROBERT H. KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Mike Qi
August 15, 2003